United States District Court
Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 17-cv-05671-BLF

ORDER CONSTRUING CLAIMS IN U.S. PATENT NOS. 7,675,806; 7,709,303; 8,004,922; 8,020,014; 8,268,672; 8,566,836

[Re: ECF 143, 158, 179]

Plaintiff VLSI Technology LLC ("VLSI") brings this patent infringement lawsuit against Defendant Intel Corporation ("Intel"), alleging infringement of eight patents, including six that are at issue in the present claim construction dispute: U.S. Patent Nos. 7,675,806 ("the '806 Patent"); 7,709,303 ("the '303 Patent"); 8,004,922 ("the '922 Patent"); 8,020,014 ("the '014 Patent"); 8,268,672 ("the '672 Patent"); and 8,566,836 ("the '836 Patent"). The Court held a tutorial on December 13, 2018 and a *Markman* hearing on December 14, 2018 ("the Hearing") for the purpose of construing ten disputed terms in the above listed patents.

I. BACKGROUND

The Asserted Patents are directed to semiconductor and microprocessor technology. VLSI asserts that Intel's products infringe the Asserted Patents. *See generally* Compl., ECF 1. Each of the six patents at issue in the present claim construction dispute is summarized below.

A. The '806 Patent

The '806 Patent is titled "Low Voltage Memory Device and Method Thereof" and was issued on March 9, 2010. Ex. 1 to Proctor Decl. ("'806 Patent"), ECF 144-1. This patent claims devices and methods for reducing power consumption in a memory system used to store data. *See id.* at 1:54–2:3; 9:16–12:8. The invention aims to reduce power consumption by employing a

high-voltage mode for storing data to a first memory and a low-voltage mode for accessing a second memory. *See id.* at 1:54–2:3. In high-voltage mode data may be stored to the first memory (a high-density memory). *Id.* at 1:58–60. In low-voltage mode the first memory may be in a data retention or sleep state and the second memory (a low-voltage memory) is capable of being accessed. *Id.* at 1:60–66. The invention can thus store data to high-density memory in high-voltage mode and access low-voltage memory in low-voltage mode. *Id.* at 1:66–2:3.

B. The '303 Patent

The '303 Patent is titled "Process for Forming an Electronic Device Including a Fin-Type Structure" and was issued on May 4, 2010. Ex. 2 to Proctor Decl. ("'303 Patent"), ECF 144-2. This patent claims processes for forming electronic devices that include fin-type transistor structures. *See id.* at 1:21–23; 8:59–10:51. The invention aims to improve the performance of fin-type transistors by providing a greater range of available channel widths to assure operation across a desired set of operating parameters. *Id.* at 1:28–33. Channel width may depend on fin height. *Id.* at 1:26–28. To enable a greater range of channel widths the patent provides a process for forming a semiconductor fin with a first height and removing a portion of the fin such that the fin is shortened to a second height. *Id.* at 1:61–65.

C. The '922 Patent

The '922 Patent is titled "Power Island with Independent Power Characteristics for Memory and Logic" and was issued on August 23, 2011. Ex. 3 to Proctor Decl. ("'922 Patent"), ECF 144-3. This patent is directed to power management and delivery in a system-on-a-chip ("SoC"). *See id.* at 1:7–2:59. An SoC is an integrated design of hardware and software components combined to form a computer on a single integrated circuit. *Id.* at 1:7–9. In SoC's, "some . . . components may be designed to operate at different power requirements, including different voltages and/or different operating frequencies." *Id.* at 1:19–22. The invention aims to reduce or save power consumption in SoC's. *See id.* at 1:46–2:59. In some embodiments, a first power characteristic to operate a memory segment is variable over a first range of power characteristics, while a second power characteristic is separately variable to operate a logic segment. *See id.* at 5:67–6:7.

D. The ’014 Patent

The ’014 Patent is titled “Method for Power Reduction and a Device Having Power Reduction Capabilities” and was issued on September 13, 2011. Ex. 4 to Proctor Decl. (“’014 Patent”), ECF 144-4. This patent claims devices and methods for reducing power consumption of components of integrated circuits. *See id.* at Abstract; 7:26–8:55. In one embodiment, the patent teaches determining whether to power down a portion of a component based on the relationship between “estimated power gain” and “estimated power loss” resulting from such powering down. *See id.* at 4:31–39; 5:37–43; 6:46–52.

E. The ’672 Patent

The ’672 Patent is titled “Method of Assembly and Assembly Thus Made” and was issued on September 18, 2012. Ex. 5 to Proctor Decl. (“’672 Patent”), ECF 144-5. This patent claims assemblies of chips—for example, a combination of a memory chip and a logic chip, or a combination of an integrated circuit and a passive chip—interconnected through solder connections and methods of assembling such interconnected chips. *See id.* at Abstract; 1:4–28; 5:6–11. The invention aims to improve the stability and reliability of interconnections between a first chip and a second chip using solder compositions and metallization. *See id.* at 1:34–53; 4:33–45. The interconnection may comprise a solder bump and an underbump metallization at the first chip and a metallization at the second chip. *See id.* at Abstract; 1:36–53; 6:46–48.

F. The ’836 Patent

The ’836 Patent is titled “Multi-Core System on Chip” and was issued on October 22, 2013. Ex. 6 to Proctor Decl. (“’836 Patent”), ECF 144-6. This patent claims a multi-core system on chip and methods for operating multi-core processor devices. *See id.* at 1:56–61; 10:44–12:47. The invention aims to improve performance of a multi-core system on chip without substantially increasing the power required by equipping the operating system to send tasks that cannot be distributed across multiple cores to the fastest available single core. *See id.* at 1:65–2:10. The invention provides for tasks that cannot be run on multiple cores to be run on the single core that has the highest operating frequency at a given operating voltage. *See id.*

II. LEGAL STANDARD

Claim construction is a matter of law. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 387 (1996). "It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude,'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citation omitted). As such, "[t]he appropriate starting point . . . is always with the language of the asserted claim itself." *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998).

Claim terms "are generally given their ordinary and customary meaning," defined as "the meaning . . . the term would have to a person of ordinary skill in the art in question . . . as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313 (internal citation omitted). The court reads claims in light of the specification, which is "the single best guide to the meaning of a disputed term." *Id.* at 1315; *see also Lighting Ballast Control LLC v. Philips Elecs. N. Am. Corp.*, 744 F.3d 1272, 1284–85 (Fed. Cir. 2014) (en banc). Furthermore, "the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim." *Phillips*, 415 F.3d at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)). The words of the claims must therefore be understood as the inventor used them, as such understanding is revealed by the patent and prosecution history. *Id.* The claim language, written description, and patent prosecution history thus form the intrinsic record that is most significant when determining the proper meaning of a disputed claim limitation. *Id.* at 1315–17; *see also Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

Evidence external to the patent is less significant than the intrinsic record, but the court may also consider such extrinsic evidence as expert and inventor testimony, dictionaries, and learned treatises "if the court deems it helpful in determining 'the true meaning of language used in the patent claims.'" *Philips*, 415 F.3d at 1318 (quoting *Markman*, 52 F.3d at 980). However, extrinsic evidence may not be used to contradict or change the meaning of claims "in derogation of the 'indisputable public records consisting of the claims, the specification and the prosecution history,' thereby undermining the public notice function of patents." *Id.* at 1319 (quoting

Southwall Techs., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1578 (Fed. Cir. 1995)).

III. DISCUSSION

At the time of the parties' joint prehearing statement the parties had not agreed on constructions for any claim terms. *See* Joint Statement at 1, ECF 118. In their joint statement the parties noted that they will "not present for construction specific terms [] that Intel asserts as indefinite, as part of the Markman process." *Id.* at 2 n.1. The Court notes that certain indefiniteness arguments were raised by Intel in its Responsive Brief. *See, e.g.*, Responsive Br. at 9 n.6., ECF 158. Any indefiniteness or other arguments raised in footnotes are not properly briefed and are denied. The Court discusses in turn the ten disputed terms.

A. Disputed terms in the '806 Patent

The parties dispute two terms in the '806 Patent: "when in a second mode of operation" and "arrangement of transistors." Both terms appear in independent claim 11 which recites:

> 11. A device, comprising:
>
> > a first memory located within an integrated circuit, the first memory having a first memory cell topology with a first minimum operating voltage, the first memory cell topology comprising a first **arrangement of transistors**;
> >
> > a second memory located within the integrated circuit, the second memory having a second memory cell topology with a second minimum operating voltage, wherein the second minimum operating voltage is less than the first minimum operating voltage and wherein the second memory cell topology comprises a second **arrangement of transistors**, the second **arrangement of transistors** different from the first **arrangement of transistors**, the second memory configured to store status information indicative of a status of data stored at the first memory; and
> >
> > a processing core located at the integrated circuit, the processing core operable to:
> >
> > > access the first memory and the second memory when in a first mode of operation, and to access the second memory but not the first memory **when in a second mode of operation**;
> > >
> > > access the status information in the second mode of operation; and
> > >
> > > enter the first mode of operation in response to the status information indicating data corresponding to the data stored at the first memory had changed.

'806 Patent at 10:31–57 (emphasis added). The term "arrangement of transistors" is also recited in claim 6. Each term is discussed in turn.

1. "when in a second mode of operation" (claim 11)

VLSI's Proposal	Intel's Proposal	Court's Construction
No construction needed because the claim already precisely defines the second mode	"when a lower voltage is provided to the first and second memory"	Plain and ordinary meaning, which includes the requirement of claim 11 that when in the second mode of operation the voltage(s) supplied to the first and second memory, respectively, must be lower than the minimum necessary for the first mode of operation

VLSI argues that no construction is necessary because "the inventors did not intend to install within this claim term the additional, incorrect limitation found in Intel's proposal that 'a lower voltage [be] provided to the first and second memory' when [the processing core is] in the second mode of operation." *See* Opening Br. at 3 (quoting Intel's proposed construction), ECF 143. Intel counters that "[d]uring prosecution, the applicant explained that the 'second mode of operation' means 'when a lower voltage is provided to the first and second memory.'" Responsive Br. at 1, ECF 158. For the reasons discussed below, the Court adopts the plain and ordinary meaning of "when in a second mode of operation" which includes claim 11's requirement that when in the second mode of operation the voltage(s) must be lower than the minimum necessary for the first mode of operation.

Indisputably, claim 11 of the '806 Patent teaches a first memory with a first minimum operating voltage and a second memory with a second minimum operating voltage "wherein the second minimum operating voltage is less than the first minimum operating voltage." *See* '806 Patent at 10:31–40. Thus, the minimum operating voltage of the second memory must be lower than the minimum of the first memory.

Claim 11 further teaches a processing core "operable to[] access the first memory and the second memory when in a first mode of operation, and to access the **second memory but not the first memory** when in **a second mode of operation**." *See* '806 Patent at 10:47–53 (emphasis added). In describing the second mode of operation, VLSI itself points to a portion of the specification that states, "the **voltage supplied to the first memory [] is reduced below its minimum operating voltage**, while the voltage supplied to the second memory [] is maintained

above the minimum operating voltage for the second memory." *See* '806 Patent at 4:32–36 (emphasis added); Opening Br. at 4. The specification further states that "**[t]he second memory . . . operates at a lower voltage than the first memory**." *See* '806 Patent at 3:58–59 (emphasis added). In other words, the specification provides that in the second mode of operation (1) the voltage supplied to the first memory is less than the minimum operating voltage of the first memory; and (2) the voltage supplied to the second memory is lower than the operational voltage of the first memory.

Put differently, when in the second mode of operation, both the voltage provided to the first memory and the voltage provided to the second memory must be lower than the minimum operating voltage of the first memory. Therefore, whether a common voltage or different voltages are provided to the first and second memory, respectively, *see id.* at 4:1–25, when in a second mode of operation the voltage must be lower than the minimum operating voltage of the first memory. Because the first mode of operation in claim 11 requires access to the first memory, the minimum voltage necessary for the first mode of operation is the minimum operating voltage of the first memory. *See id.* at 10:47–52.

Accordingly, the second mode of operation requires that the operating voltage of the second memory is lower than the minimum operating voltage of the first memory in order to "access the **second memory but not the first memory**." *See id.* at 10:50–51 (emphasis added). If in the second mode of operation the voltage was equal to or greater than the minimum operating voltage of the first memory, access to the first memory would not be restricted as required by the claim language.

At the Hearing, the Court proposed a construction consistent with that adopted here, to which Intel did not object. *See* Hearing Transcript at 27:23–28:17, 30:13–24. Also at the Hearing, VLSI acknowledged that no embodiments of the patent contemplate that when in the second mode of operation the voltage can be higher than the minimum required for the first mode. *See id.* at 32:9–19. For these reasons and due to the Court's construction, the Court need not and does not address the parties' additional arguments.

In sum, the Court adopts the plain and ordinary meaning of the disputed term "when in a

second mode of operation," which includes the requirement of claim 11 that when in the second mode of operation the voltage(s) supplied to the first and second memory, respectively, must be lower than the minimum necessary for the first mode of operation.

2. "arrangement of transistors" (claims 6 and 11)

VLSI's Proposal	Intel's Proposal	Court's Construction
No construction needed because the term as selected by the inventors requires no clarification	"number of transistors and connectivity among those transistors"	"arrangement of PMOS and/or NMOS transistors defined by the total number of transistors, number of PMOS or NMOS transistors, and manner of connection between the transistors"

In its briefing VLSI argued that no construction was necessary for the term "arrangement of transistors" while Intel argued that the term is defined according to the "number of transistors and connectivity among those transistors." *See* Opening Br. at 6; Responsive Br. at 5. However, at the Hearing, the parties agreed that three factors inform a given "arrangement of transistors": transistor type, the number of transistors, and the manner of connection between the transistors. *See* Hearing Transcript at 20:7–24, 35:2–4. The parties further agreed that transistor size does not inform an arrangement of transistors. *See id.* at 33:8–20, 36:12–16. In other words, the parties agreed that if the only difference between two transistor layouts was transistor size then the two layouts would constitute the same "arrangement of transistors."

The only remaining dispute is whether to further narrow the meaning of transistor type. Intel argued at the Hearing that transistor type should be limited to "PMOS or NMOS" while VLSI argued that transistor type should not be defined. *See id.* at 36:6–17. The Court agrees with Intel. VLSI acknowledges that "the sorts of transistors discussed in the patent each fall into one of two kinds: 'p-MOS' and 'n-MOS.'" *See* Opening Br. at 6. Thus, limiting transistor type to PMOS[1] or NMOS is consistent with the '806 Patent and stands only to add clarity. Accordingly, here, transistor type is properly limited to PMOS or NMOS.

Based on the foregoing, the Court adopts the following construction: "arrangement of PMOS and/or NMOS transistors defined by the total number of transistors, number of PMOS or

[1] The parties interchangeably use "PMOS" and "p-MOS"; "NMOS" and "n-MOS."

NMOS transistors, and manner of connection between the transistors."

B. Disputed term in the '303 Patent

1. "height" (claims 1, 8, 11, 12, 18 and 19)

VLSI's Proposal	Intel's Proposal	Court's Construction
"a distance measured in a direction substantially perpendicular to a major surface of a substrate"	"physical dimension of distance from the base to the top of a structure in a direction substantially perpendicular to a surface from which a transistor structure is subsequently formed"	"physical dimension of distance from the base to the top of a structure in a direction substantially perpendicular to the primary surface"

The term "height" appears in multiple claims of the '303 Patent. Claim 1 is representative and recites:

> 1. A process for forming an electronic device comprising:
>
> forming a first semiconductor fin for a first fin-type transistor structure over a support layer of a substrate, wherein, the first semiconductor fin has a first **height**; and
>
> removing a portion of the first semiconductor fin to provide the first semiconductor fin with a second **height**, wherein the second **height** is smaller than the first **height**.

'303 Patent at 8:60–67 (emphasis added).

The parties agree that "height" as used in the patent corresponds to a distance measured in a direction substantially perpendicular to a major substrate surface but dispute whether the patent limits a single fin to a single height. VLSI argues that "the height of a fin [] can be location-dependent," *see* Opening Br. at 9, while Intel counters that the fins claimed by the '303 Patent are defined by only "a single height at a time," *see* Responsive Br. at 9. On its face, VLSI's proposed construction would permit the same fin to have multiple "heights" while Intel's proposed construction would not. As an analogy, VLSI's construction could define a person by two heights—one from the ground to the shoulders and one from the ground to the crown of the head—whereas Intel's construction would define the person's height by only the latter.

"[T]he specification may reveal a special definition given to the claim by the patentee that differs from the meaning it would otherwise possess." *Phillips*, 415 F.3d at 1316. Such lexicography governs where it "clearly set[s] forth a definition of the disputed claim term" and

"clearly expresses an intent to define the term." *See GE Lighting Solutions, LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) (internal quotations and citation omitted). Here, in support of their respective proposed constructions, VLSI and Intel each argue that a different definition of "height" in the specification controls. VLSI advances the following definition found in column 3 of the specification:

> Note the term "height" is understood herein to refer to a distance measured in a direction substantially perpendicular to a major surface of substrate **12**.

'303 Patent at 3:3–6; *see also* Opening Br. at 8. Meanwhile, Intel advances the following definition found in column 6 of the specification:

> As used herein, the term "height" is intended to mean the physical dimension of distance from the base to the top of a structure in a direction substantially perpendicular to the primary surface.

'303 Patent at 6:21–24; *see also* Responsive Br. at 7. For the reasons discussed below, the Court construes the term "height" according to the definition appearing at column 6, lines 21 to 24.

Patentee's definition of "height" at column 6 is the only one of the two that governs under *GE Lighting*. Although both definitions are "clearly set forth," *see GE Lighting*, 750 F.3d at 1309, patentee "clearly expresse[d] an intent to define the term" with respect to the definition at column 6 only, *see id.* "Height" at column 6, lines 21 to 24, is "defined . . . to aid **in understanding this specification**." *See* '303 Patent at 5:61–62 (emphasis added); *see also id.* at 6:21–24. In other words, the definition of height at column 6 appears within the section of the specification dedicated to defining terms as they apply to the entire specification. *See id.* at 5:60–6:52. Meanwhile, "height" as defined at column 3, lines 3 to 6, appears within a paragraph of the specification dedicated only to describing Figure 3 of the patent. *See id.* at 2:56–3:13.

Moreover, "[t]he patentee's lexicography must . . . appear with reasonable clarity, deliberateness, and precision before it can affect the claim." *Abbott Laboratories v. Syntron Bioresearch, Inc.*, 334 F.3d 1343, 1354 (Fed. Cir. 2003) (internal quotation and citation omitted) (emphasis removed). The definition at column 3 states, "the term 'height' is **understood herein** to refer to . . . a major substrate of surface **12**," *see* '303 Patent at 3:3–6 (emphasis added), but the scope of the word "herein" is unclear. The explicit reference to "a major substrate of surface **12**"

indicates that "herein" as used at column 3, line 4, corresponds only to Figure 3. *See id.* at 6:1–13. By comparison, the definition of "height" at column 6, lines 21 to 24, corresponds specifically to "understanding this specification," *see id.* at 5:60–61. The Court is simply not persuaded that patentee's definition of "height" at column 3 referring to a figure in a paragraph dedicated to describing that figure provides the requisite "clarity, deliberateness, and precision," *see* Abbott, 334 F.3d at 1354, to overcome patentee's explicit definition of "height" at column 6 with respect to the entire specification.

VLSI argues that "any construction of 'height' must be consistent with the patent's usage of that term" and that "only VLSI's proposed construction satisfies th[is] requirement." *See* Opening Br. at 10. The Court disagrees that only VLSI's proposal is adequate. VLSI's proposed construction would permit the same fin to have multiple "heights" at a given time, which is not supported by the specification or the claims. Instead, the patent contemplates fins having only a singular "height" at a given time. *See, e.g.*, '303 Patent at 8:61–67 ("forming a first [] fin . . . ha[ving] a first height"); 1:64–65 ("removing a portion of the [] fin such that the [] fin is shortened to a second height"); 9:46–47 ("provid[ing] the third [] fin with a third height"). In other words, the patent claims fins with only one height at one time. Thus, the Court finds no inherent conflict between the definition of "height" at column 3 which describes "the [] value as the 'thickness' of the previously formed layer **18** [a fin]," *see id.* at 3:1–3, and the definition of "height" at column 6 which would provide the same measurement. VLSI admits that all examples of fins disclosed in the patent have a single height. *See* Opening Br. at 9. The Court recognizes that a patent's claims are not limited to illustrated embodiments, *see Electro Sci. Indus., Inc. v. Dynamic Details, Inc.*, 307 F.3d 1343, 1348–49 (Fed. Cir. 2002); however, the Court does not find support for VLSI's proposed construction in the claims themselves. Accordingly, the Court finds that the definition of "height" at column 3 does not demonstrate additional breadth of the term. *Cf. Prima Tek II, L.L.C. v. Polypap, S.A.R.L.*, 318 F.3d 1143, 1151 (Fed. Cir. 2003).

VLSI additionally argues that the definition of "height" at column 6 is inapposite because in the same section the specification states, "top . . . [is] intended to clarify [a] relative position[] within an illustration unless expressly defined otherwise." *See* '303 Patent at 6:5–7; Opening Br.

at 9. This argument fails. For one, "height" as defined in column 6 is the controlling definition for the reasons stated above, regardless of whether one or more of the words used in the definition is defined elsewhere. Second, the definition of height in column 6 does not refer to "an illustration," but instead to the entire specification. *See* '303 Patent at 5:61–62; 6:21–24. Accordingly, the patentee's definition of "top" does not alter the Court's construction of the term "height."

Finally, the Court declines to adopt the portion of Intel's proposed construction that would replace "the primary surface" phrase of column 6's definition of height with "a surface from which a transistor structure is subsequently formed." *See* Responsive Br. at 7. The term "primary surface" is defined in the specification and needlessly stacking definition upon definition does not serve to clarify the claim language.

In sum, the Court construes the term "height" to mean "physical dimension of distance from the base to the top of a structure in a direction substantially perpendicular to the primary surface."

C. Disputed term in the '922 Patent

1. "conversion controller coupled to the supply power converter" (claims 1 and 11)

VLSI's Proposal	Intel's Proposal	Court's Construction
"conversion controller (which is further described later in the claim) coupled to the supply power converter (which was introduced earlier in the claim)"	"conversion controller that is separate from the supply power converter"	"conversion controller coupled to but separate from the supply power converter"

The parties contest the meaning of the term "conversion controller coupled to the supply power converter" in claims 1 and 11 of the '922 Patent. Claim 1 is representative and recites:

> 1. A power island for a system-on-a-chip (SoC), the power island comprising:
>
> > . . . a supply power converter coupled between the supply line and the scalable logic, wherein the supply power converter is configured to convert a supply voltage of the external supply signal from the first power characteristics to the second power characteristics; and
> >
> > a **conversion controller coupled to the supply power converter**, wherein the conversion controller is configured to control the supply power converter to change the external supply signal according to the second power characteristics of the scalable logic.

'922 Patent at 9:9–37 (emphasis added).

As an initial matter, at the Hearing, Intel confirmed that its alternative proposed construction "conversion controller **that is separate from** the supply power converter," *see* Responsive Br. at 11 (emphasis added), is the "current state of play," *see* Hearing Transcript at 62:2–4. Also at the Hearing, VLSI confirmed that it is seeking simply the claim language "conversion controller **coupled to** the supply power converter." *See* Hearing Transcript at 55:10–11 (emphasis added). Thus, the only difference between the parties' proposed constructions is whether the conversion controller must be "separate" from the supply power converter or merely "coupled to."

That being said, the discussion at the Hearing made clear that this dispute is somewhat of a mirage—based on their representations at the Hearing, the parties do not actually disagree in a significant way. Intel argues that during prosecution the applicant overcame the prior art by including "the requirement that the conversion controller be 'separate' [from the supply power converter]." *See* Responsive Br. at 10; *see also* Hearing Transcript at 58:15–61:20. Intel contends that therefore the words "coupled to" as used in the term are properly construed to mean "that is separate from." *See* Responsive Br. at 11.

At the Hearing, VLSI repeatedly acknowledged that the conversion controller and supply power converter are "separate elements." For example, VLSI explained that "[the conversion controller and supply converter] are coupled together, they are recited as separate elements." *See* Hearing Transcript at 52:22–53:2. VLSI admitted that "coupling is a connection **of two things**, it's not a merging into one." *See id.* at 53:3–9 (VLSI agreeing with the Court's description) (emphasis added). VLSI further explained that "[w]hen things are coupled together . . . there's **still separately recited elements**, and whenever we apply the claims, we still have to find the conversion controller. We still have to find the supply power converter." *See id.* at 54:18–22 (emphasis added). VLSI recapped by stating, "as emphasized earlier, there are **separately recited elements**." *Id.* at 58:5–7 (emphasis added).

Thus, the Court finds no meaningful dispute over the "separate from" requirement itself. Instead, VLSI takes issue with what Intel's proposed construction would write out of the claim—

the "coupled to" language. *See* Hearing Transcript at 58:6–12 (VLSI stating, "We are not suggesting that we can cut one of those [separately recited] elements out in any way, we simply want to remain faithful to the claim . . . . Intel's proposed construction[] deviates at least a little bit from what the original claim said."). In other words, VLSI does not agree that "coupled to" is properly *replaced with* "separate from." *See id.* at 54:24–55:1. The Court agrees that Intel's proposed construction is not consistent with the claims because Intel's proposed phrase "that is separate from" does not fully describe the "coupled to" claim language. Put differently, the conversion controller and supply power converter could exist separate from another, without being coupled to one another. For example—as discussed at the Hearing by VLSI—a wire may "couple" together the two separate elements. *See* Hearing Transcript at 57:12–22. But, if not for the wire, the conversion controller and supply power converter would be "separate from" but not "coupled to" each other. This scenario is not contemplated by the claims but would pass under Intel's proposed construction. Therefore, Intel's proposed construction would impermissibly read out an aspect of "coupled to."

Accordingly, for the reasons discussed above, the Court finds it appropriate to maintain the "coupled to" claim language while clarifying that the two elements are "separate from" each other. Although the parties dispute whether the applicant's statements during prosecution mandate the "separate from" limitation, this disagreement is moot over VLSI's representations at the Hearing and the Court's construction.

In sum, the Court construes the disputed term to mean "conversion controller coupled to but separate from the supply power converter."

D. Disputed term in the '014 Patent

1. "estimated power loss" (claims 1 and 12)

VLSI's Proposal	Intel's Proposal	Court's Construction
"estimated loss of power"	"a power consumption estimate made during the integrated circuit's / device's operation"	No construction necessary

The disputed term "estimated power loss" appears in claims 1 and 12 of the '014 Patent. Claim 1 is representative and recites:

1. A method for power reduction, the method comprising:

> selectively providing power to at least a portion of a component of an integrated circuit during a lower power mode; and
>
> determining whether to power down the at least portion of the component in response to a relationship between an estimated power gain and an **estimated power loss** resulting from powering down the at least portion of the component during the lower power mode.

'014 Patent at 7:27–35 (emphasis added). The "estimated power gain" may correspond to the power saved or not used due to powering down. *See id.* at 5:52–57. Meanwhile, the "estimated power loss" may correspond to operations required prior to powering up or down—operations which themselves may require power equal to or exceeding the "power gain" from powering down. *See id.* at 3:35–38; 6:49–52. The patent teaches powering down "if the power gain is greater than the power loss." *Id.* at 6:49–50.

As an initial matter, the Court notes that Intel's proposed construction is the alternative construction proposed by Intel to "narrow the disputes." *See* Responsive Br. at 12 n.9; *see also* Hearing Transcript at 70:7–11. The parties contest two remaining points: (1) whether "loss" should be replaced with "consumption"; and (2) whether the estimate of power loss must be made *during* the operation of the integrated circuit / device. *See* Opening Br. at 13; Responsive Br. at 12. The Court addresses each point in turn.

First, VLSI contends that "the concept of 'power loss' as recited in the claim is not the same as the concept of 'power consumption,' which is [Intel's proposal]." *See* Opening Br. at 13. In support, VLSI argues that the patent distinguishes power loss from consumption, *see id.*, pointing out that the patent expressly states**, "the power loss** . . . can be evaluated in response to various parameters that affect the **power consumption** rate," *see* '014 Patent at 7:10–12 (emphasis added). Intel counters that a person of ordinary skilled in the art ("POSITA") would understand "power loss" to refer to an electronic device "consuming power" not "losing power." *See* Responsive Br. at 12. Intel also points out that the patent states, "**power loss** indicates the **power consumed** during information retrieval operation . . . ." *See* '014 Patent at 6:32–35 (emphasis added).

The Court agrees with VLSI that it would be improper to replace "power loss" with

"power consumption." Intel argues that "power consumption" would "help[] the jury understand the term." *See* Responsive Br. at 12. However, the words of the claim must be understood as the inventor used them. *See Phillips*, 415 F.3d at 1316. Here, the patentee drew a distinction between "power loss" and "power consumption"—both terms are used in the specification, but not interchangeably. For example, the specification uses "power consumption" to generally describe "various power consumption control techniques [previously] suggested," s*ee* '014 Patent at 2:19–21, and to explain that "[u]sually power consumption can vary more dynamically when a larger number of segments or lines is involved," *see id.* at 4:20–22. On the other hand, the specification uses "power loss" specifically with respect to the claimed invention—e.g., "a power loss associated with powering down the at least portion of the component." *See id.* at 6:29–31. Moreover, while "the power loss . . . **can be evaluated** in response to various parameters that affect the power consumption rate," *see id.* at 7:10–12 (emphasis added), the patent contemplates power loss that is not necessarily quantified as power consumption, *see id.* at 6:56–7:2 (determining whether to power down based on "the amount of dirty bits"). Finally, "power consumption" is not used in the claims. *See id.* at 7:27–35; 8:8–18. In sum, the Court finds no reason to depart from the inventor's selection of "power loss." *See Phillips*, 415 F.3d at 1316.

Second, VLSI argues that the term "estimated power loss" does *not* include a "temporal limitation," *see* Opening Br. at 14, while Intel contends that power loss can only be estimated "*during* the integrated circuit's/device's[2] operation," *see* Responsive Br. at 13 (emphasis in original). Intel maintains that "the 'power loss' referred to in the specification ***varies during*** the operation of a component of the integrated circuit/device, and therefore can only be 'estimated' ***during*** . . . operation." *See* Responsive Br. at 13 (emphasis in original). In support, Intel points out that every parameter the specification discloses as affecting "power loss" varies during the operation of the integrated circuit/device. *See id.* at 13–14 (citing '014 Patent). VLSI counters that the claims include no such limitation and that "[s]imply because power loss might vary during operation does not mean it cannot be estimated in advance," *see* Reply Brief at 8.

[2] Claim 1 of the '014 Patent refers to an "integrated circuit" while claim 12 refers a "device."

The Court finds that Intel's proposed limitation "during the integrated circuit's / device's operation" is not warranted. Intel's argument essentially boils down to an assertion that the embodiments disclosed in the '014 Patent do not describe "estimated power loss" except during operation of the integrated circuit/device. *See* Responsive Br. at 13–14. Even if true, such an argument on its own does not mandate inclusion of Intel's proposed limitation. *See Electro Sci.*, 307 F.3d at 1348–49 ("A Court may not import limitations from the written description into the claims.") (internal quotation and citation omitted). Indeed, "[t]he specification need not describe every embodiment of the claimed invention, and the claims should not be confined to the disclosed embodiments—even when the specification discloses only one embodiment." *Woods v. DeAngelo Marine Exhaust, Inc.*, 692 F.3d 1272, 1283 (Fed. Cir. 2012).

Intel represents that "the specification expressly states that 'estimated power ***gain***'—unlike 'estimated power ***loss***'—can be predefined." *See* Responsive Br. at 14 (citing '014 Patent at 5:64–67) (emphasis in original). However, review of column 5, lines 64 to 67, reveals that the specification simply states, "[a]ccording to an embodiment . . . the power gain is predefined." *See id.* Contrary to Intel's suggestion, the specification does *not* expressly or otherwise state that power *loss* could not be predefined—instead, the specification is silent on this point. Thus, the Court turns to the claims themselves, and finds no grounds for imposing Intel's proposed limitation. Claims 1 and 12 do contain a temporal limitation ("during a low power mode," *see, e.g.*, '014 Patent at 7:35), but nothing of the sort suggested here by Intel. The Court is unwilling to read in the proposed limitation "during the integrated circuit's / device's operation" based on examples in the specification. *See Woods*, 692 F.3d at 1283.

In sum, the Court finds that construction of the disputed term "estimated power loss" is not necessary or warranted.

E. Disputed term in the '672 Patent

1. "bumps . . . on top of the solder composition | solder interconnection layer" (claims 3 and 12)

VLSI's Proposal	Intel's Proposal	Court's Construction
"bumps . . . above the solder composition | solder interconnection layer"	"solder . . . on the surface of the solder composition | solder interconnection layer"	"solder bumps. . . on top of the solder composition | solder interconnection layer"

		where "on top of" includes the requirement that the solder bumps must be in contact with the solder composition | solder interconnection layer

The disputed term "bumps . . . on top of the solder composition | solder interconnection layer" appears in claims 3 and 12 of the '672 Patent. The two claims are as follows:

> 3. A method as claimed in claim 1, wherein the first chip is provided with further **bumps** of a larger height **on top of the solder composition**, said first chip extending laterally beyond the second chip.
>
> . . .
>
> 12. An assembly as claimed in claim 9, wherein the first chip extends laterally beyond the second chip and is provided with **bumps** that are present **on top of the solder interconnection layer**.

'672 Patent at 8:23–26, 10:1–4 (emphasis added). The parties' disagreement concerns only the first four words of the disputed term—"bumps . . . on top of," *see id.*

VLSI proposes "**bumps . . . above** the solder composition," *see* Opening Br. at 15 (emphasis added), while Intel proposes "**solder . . . on the surface of** the solder composition," *see* Responsive Br. at 15 (emphasis added). Thus, the parties' disagreement is twofold : (1) whether to use "bumps" or "solder" and (2) whether to use "above" or "on the surface of." *See id.* The Court addresses each dispute in turn.

First, VLSI argues that "not all bumps are solder," that "not all solder is shaped like a bump," and that "'bumps' is a plural term, whereas 'solder' is singular." *See* Opening Br. at 16. VLSI contends that therefore, substituting "solder" for "bumps" would "alter, not explain, the claims." *Id.* Intel counters that based on the claims and the specification "a POSITA would readily understand that the 'bumps' of claims 3 and 12 are an additional solder on the surface of the solder composition/interconnection layer." *See* Responsive Br. at 17.

The Court finds that the claims dictate that the "bumps" must be composed of solder, i.e. "solder bumps." As VLSI recognizes, "the claims of the patent, not its specification, measure the invention." *See* Reply Br. at 9 (quoting and citing *Smith v. Snow*, 294 U.S. 1, 11 (1935)). Here, bumps are mentioned in the claims for the first time as "**further** bumps" in dependent claim 3.

See '672 Patent at 8:23–26 (emphasis added). Dependent claim 3 relies on independent claim 1, which recites the following elements: "first chip," "second chip," "bond pads," "solder composition," "underbump metallization," "metallization," and "intermetallic compound." *See id.* at 8:2–19. Of these elements, the only antecedent basis for the "further bumps" of claim 3 is the "solder composition" of claim 1—a point VLSI acknowledged at the Hearing, *see, e.g.*, Hearing Transcript at 99:5–10. VLSI admitted that "a particular bump can be solder, it can be made out of solder composition." *See id.* at 99:5–6. Put differently, the "solder composition" of claim 1 may be a bump of solder and would therefore provide an antecedent basis for the "further bumps" of claim 3—but necessarily *only where* the "further bumps" are made of solder. Accordingly, the Court finds that "bumps" as used in the claims of the '672 Patent means "solder bumps," which retains the claim language while incorporating the necessary "solder" limitation.

Second, VLSI argues that "on top of" as used in claims 3 and 12 permits "one element [to be] above (but physically spaced apart from) another." *See* Opening Br. at 17. Intel proposes that "the phrase 'on top of' should be construed as 'on the surface of' the claimed solder composition layer." *See* Responsive Br. at 16. Intel seeks this construction because it contends the "bumps" of claims 3 and 12 "are ***in physical contact*** with, and thus on the surface of, the [] solder composition." *See id.* (emphasis in original). Indeed, the crux of this dispute is whether the "further [solder] bumps" must be in contact with the solder composition of claim 3 and solder interconnection layer of claim 12. *See* Hearing Transcript at 80:17–81:1; 88:20–23.

The Court finds that the phrase "on top of" includes the requirement that the solder bumps be in contact with the solder composition/interconnection layer. VLSI's proposed construction would permit the "further [solder] bumps" of claims 3 and 12 to be physically untethered from the solder composition/interconnection layer below. A plain reading of the claims prohibits this construction. Claim 1 sets forth providing bonds pads that have "underbump metallization" at a surface of a first chip. *See* '672 Patent at 8:2–6. Claim 1 further requires that "solder composition is provided . . . on the underbump metallization." *Id.* at 8:14–15. In other words, the solder composition is the top layer of the first chip/bond pad/underbump metallization/solder composition stack. In claim 1, the solder composition connects the first and second chips. *See id.*

at 8:12–19. Dependent claim 3 requires that the first chip be provided with "further [solder] bumps of a larger height *on top of* the solder composition, said first chip *extending laterally beyond* the second chip." *Id.* at 8:23–26 (emphasis added). To have a larger height, the "further [solder] bumps of a larger height" are necessarily on the portion of the first chip "extending laterally beyond the second chip." *See id.* at 8:2–26. Thus, in being "on top of" the solder composition the "further [solder] bumps" must be in contact with the solder composition. The claims simply do not contemplate another location through which the "further [solder] bumps" could be "[provided to] the first chip." *See id.* at 8:23–26. A similar analysis applies to claim 12, which is dependent on claim 9.

VLSI relies on Figure 1A of the patent for the proposition that there may be a gap between the solder bumps and solder composition/interconnection layer. *See* Opening Br. at 15–16. VLSI argues that because elements 23 and 26 in Fig. 1A are separated by a gap, the claims contemplate gaps between the solder bumps and solder composition/interconnection layer of claims 3 and 12. *See id.* This argument is misguided. In Fig. 1A, element 26 is a "deposited solder dot" on a "lead frame 10." *See* '672 Patent at 6:11–27. Elements 14 and 15 are "conductive interconnections" and elements 16 and 17 are "contact surfaces." *See id.* Thus, the gap in Fig. 1A between elements 23 and 26 simply has nothing to do with claims 3 and 12, which pertain to a method of assembly of a first *chip* and second *chip*, and assembly of a first *chip* and second *chip*, respectively. Accordingly, the Court is not persuaded that the "gap" in Fig. 1A referenced by VLSI teaches that the solder bumps in claims 3 and 12 are not in contact with the solder composition/interconnection layer.

VLSI additionally argues that other patents use the term "on top of" to refer to "two structures [that] are physically separated," and that therefore the term should be construed similarly here. *See* Opening Br. at 16. This argument is unconvincing. VLSI has not shown that these "other patents" are related to the '672 Patent or that the other patents describe solder bumps "on top of" a solder composition or interconnection layer. Finally, contrary to VLSI's suggestion, *see* Opening Br. at 17, "on top of" and "above" are not synonyms. Given two objects, for one to be "on top of" the other implies contact between the objects, while "above" does not. As a

rudimentary example, given a lamp and a table, to say the lamp is "on top of" the table would require contact, whereas to say the lamp is "above" the table would not. If the lamp were suspended above the table, it would not be "on top of" the table.

Notwithstanding the foregoing, the Court is not convinced that Intel's proposed construction "on the surface of" is proper due to inconsistencies between "on the surface" and "on top of." However, Intel is only effectively seeking a requirement the solder bumps must be in contact with the solder composition/interconnection layer, which the Court has found. Thus, the Court declines to adopt Intel's proposed construction "on the surface of."

In sum, the Court construes the disputed term "bumps . . . on top of the solder composition | solder interconnection layer" as "solder bumps. . . on top of the solder composition | solder interconnection layer." The phrase "on top of" includes the requirement that the solder bumps must be in contact with the solder composition | solder interconnection layer.

F. Disputed terms in the '836 Patent

Initially, the parties disputed four terms in the '836 Patent—three so-called "task" terms in claims 1, 10 and 20, and the term "running a multi-core application on a plurality of the multiple cores" in claim 20. However, at the Hearing, Intel agreed with VLSI's proposed alternative constructions for the "task" terms in claims 1 and 20. *See* Hearing Transcript at 114:12–18; Opening Br. at 17. The Court accordingly approves and adopts the following constructions:

Term	Agreed Construction
"upon identifying a processing task that can not be run across the plurality of cores" ('836 Patent, claim 1)	"upon identifying a single-core task"
"upon identifying a processing task that cannot be run across the plurality of the multiple cores" ('836 Patent, claim 20)	"upon identifying a single-core task"

Thus, only two terms in the '836 Patent remain in dispute: (1) "a processing task that can not be run across the plurality of cores"; and (2) "running a multi-core application on a plurality of the multiple cores." Each term is discussed in turn.

1. "a processing task that can not be run across the plurality of cores" (claim 10)

VLSI's Proposal	Intel's Proposal	Court's Construction
"a single-core task"	"in response to determining that a processing task requires a single core to run" Alternatively: "a single-core task upon identifying said task"[3]	"a single-core task upon identifying said task"

Claim 10 of the '836 Patent recites:

10. A multi-core system on chip (SOC), comprising:

> a plurality of cores, each core comprising a performance measurement circuit for measuring a performance parameter value for said core; and
>
> at least a first storage device for storing the performance parameter values for the plurality of cores for use in selecting a core having maximized or minimized performance parameter value at a specified voltage to run **a processing task that can not be run across the plurality of cores**.

'836 Patent at 11:20–29 (emphasis added).

This term is the same as the agreed-upon term in claim 1 of the '836 Patent except this term does not contain the "upon identifying" claim language. Indeed, the phrase "upon identifying" does not appear in claim 10 of the '836 Patent, leading to the instant dispute—Intel contends that "upon identifying" nonetheless applies to claim 10, whereas VLSI contends it does not. VLSI argues that claim 10 is "an apparatus claim, not a method claim," directed to "[a] multi-core system on chip (SOC)" comprising certain elements. *See* Opening Br. at 19; '836 Patent at 11:20–29. VLSI asserts that "Intel [] seeks to inject method limitations into this apparatus claim," and that the claim language says "nothing about how or when anything is 'determining' anything . . . . [or] 'in response to' anything." *See* Opening Br. at 19. Intel counters that the "applicants' statements during prosecution make clear that the 'upon identifying' phrase [of claims 1 and 20] also applies to claim 10." *See* Responsive Br. at 20.

Prosecution disclaimer precludes a patentee from recapturing a specific meaning that was previously disclaimed during prosecution. *Omega Eng'g, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1325–26 (Fed. Cir. 2003). For prosecution disclaimer to attach, "disavowing actions or statements

[3] As proposed by Intel at the Hearing. *See* Hearing Transcript at 114:20–115:5.

made during prosecution [must] be both clear and unmistakable." *Id.* According to Intel, the "applicants made repeated assertions that ***each of*** claims 1, 10, and 20 require 'identifying' a processing task that cannot be run across cores." *See* Responsive Br. at 22 (emphasis in original). In Intel's view, the applicants disclaimed a broader interpretation of claim 10—that is, similar to claims 1 and 20, "claim 10 must also be construed to require ***identification*** of a processing task that cannot be run across the plurality of cores." *See id.* at 22–23 (emphasis in original). On the other hand, VLSI contends that Intel "presents [] quotes out of context," and urges the Court to read beyond Intel's "heavily edited, out-of-context prosecution history excerpts." *See* Reply at 10–11.

Claim 10 is an apparatus claim that recites the functional limitation "to run a processing task" but does not explicitly require "identification" of the processing task. *See* '836 Patent at 11:20–29. Intel relies on three prosecution history statements by the applicants to support its theory of prosecution disclaimer. *See* Responsive Br. at 22–23 (citing 7/25/12 Amendment at 7, Ex. 12 to Selwyn Decl., ECF 158-13; 7/25/12 Amendment at 8; 7/2/13 Notice of Allowance at Bates number VLSI00001934, Ex. 12 to Selwyn Decl., ECF 158-13). For the reasons discussed below, the Court finds that the applicants clearly and unmistakably represented to the Examiner that "identification" is a requirement of claim 10 and therefore disclaimed any reading that does not include that requirement.

To overcome rejection of claims 1 to 19 during prosecution, the applicants explained to the examiner that:

> [T]he claims **require identification** of **"a processing task** that can not be run by the plurality of cores." *See, e.g.*, **claim 1** ("**upon identifying a processing task** that can not be run by the plurality of cores . . . ") and **claim 10** (" . . . **to run a processing task** that can not be run by the plurality of cores").

See 7/25/12 Amendment at 8 (emphasis added and removed). The proposed language of claim 10 in the 7/25/12 Amendment does not differ from claim 10 of the '836 Patent in any way relevant to the instant dispute.[4] Thus, the applicants explicitly admitted that claim 10 "**require[s]**

[4] Claim 10 of the '836 Patent only adds "at a specified voltage" and replaces "by" with "across," compared to the proposed language of claim 10 in the 7/25/12 Amendment.

identification of a processing task"—the applicants state that the claims include this requirement, and use claim 10 as an explicit example of such a claim. *See id.* (emphasis added). The Court cannot interpret this statement as anything but "clear and unmistakable." *See Omega*, 334 F.3d at 1326. VLSI acknowledges that in making this statement the applicants "did address the claim language," but argue that the applicants were simply "explaining that the [E]xaminer had misapprehended the claims by confusing tasks with cores." *See* Reply Br. at 11. While true that the applicants were discussing "identification of cores" vs. "identification of a processing task," *see* 7/25/12 Amendment at 8, this does nothing to limit the applicants' clear and unmistakable admission that claim 10 requires "identification," *see id.*

The applicants' statement quoted above is a clear and unmistakable disavowal of a broader interpretation of claim 10 and on its own sufficient to find prosecution disclaimer. That being said, multiple additional statements by the applicants lend further support to the Court's finding. For example, the applicants attempt to distinguish claims 1 and 10 from the prior art by arguing that "there is no teaching or suggestion by [the prior art] **of identifying tasks** 'that can not be run by the plurality of cores.'" *See* 7/25/12 Amendment at 8 (emphasis added). In other words, the applicants relied on claim 10's implicit requirement of "identification" to overcome the prior art. *See id.*; 7/2/13 Notice of Allowance at Bates number VLSI00001934. As another example, the applicants stated that "***upon identifying*** a single-core processing task that cannot be run by the plurality of cores, the core having the fastest measured processing speed parameter is selected to run the identified single-core processing task. ***See, e.g., claims 1, 10, and 20***." *See* 7/25/12 Amendment at 7, Ex. 12 to Selwyn Decl. (emphasis added).

VLSI's counterarguments are unavailing. Contrary to VLSI's assertion, *see* Opening Br. at 19; Reply at 11, the Court is not "rewriting" claim 10 but instead clarifying that claim 10 includes the same "upon identifying" requirement that the applicants clearly and unmistakably admitted it did during prosecution. In addition, the Court's construction does not inject a method step into an apparatus claim, but merely "defin[es] [] part of [the] invention in functional terms." *See Yodlee, Inc. v. CashEdge, Inc.*, 2006 WL 3456610, at *4 (N.D. Cal. Nov. 29, 2006). "There is nothing inherently wrong with defining some part of an invention in functional terms. Function

language does not, in and of itself, render [an apparatus] claim improper." *Id.* (internal quotation and citation omitted).

In sum, the Court construes the disputed term "a processing task that can not be run across the plurality of cores" in claim 10 as "a single-core task upon identifying said task," which incorporates the necessary identification requirement and maintains consistency with the parties' agreed-upon constructions.

2. "running a multi-core application on a plurality of the multiple cores" (claim 20)

VLSI's Proposal	Intel's Proposal	Court's Construction
No construction needed because the terms are readily understood	"in response to determining that an application requires a plurality of the multiple cores to run, running the application on the plurality of the multiple cores"	No construction necessary

Claim 20 of the '836 Patent recites:

> 20. In a multi-core processor comprising multiple cores which are controlled by system logic, a method for executing single core applications and multi-core applications comprising:
>
> measuring a maximum processing speed value for reach of the multiple cores for at least a first operating voltage;
>
> storing each measured maximum processing speed value for reach of the multiple cores;
>
> **running a multi-core application on a plurality of the multiple cores** by controlling each of the plurality of the multiple cores to run at a speed which is identified from the stored maximum processing speed values to be the slowest maximum processing speed of the plurality of the multiple cores; and
>
> running a single core application on a single core which is identified from the stored maximum processing speed values for the multiple cores as being the fastest core upon identifying a processing task that cannot be run across the plurality of the multiple cores.

'836 Patent at 12:16–35 (emphasis added).

VLSI argues that no construction is necessary, *see* Opening Br. at 24–25, while Intel contends that "the claimed method must first *determine* whether an application is a multi-core application" in order to execute that type of application on multiple cores, *see* Responsive Br. at 24 (emphasis added). Intel acknowledges that claim 20 recites no such explicit requirement but

argues that the requirement is implicit in the claim, specification, and prosecution history. *See id.* at 24–25. For the reasons stated below, the Court finds that no construction is necessary and that the plain and ordinary meaning of the term "running a multi-core application on a plurality of the multiple cores" controls.

"[C]laim terms must be given their plain and ordinary meaning to one of skill in the art." *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1367 (Fed. Cir. 2012). A "patentee is free to choose a broad term and expect to obtain the full scope of its plain and ordinary meaning unless the patentee explicitly redefines the term or disavows its full scope." *Id.* On its face, claim 20 does *not* include the limitation proposed by Intel and the Court does not find sufficient support in the remainder of the intrinsic record to implicitly read in such a requirement.

Intel asserts that because claim 20 runs a single core application "upon identifying a [single-core task]," there must be an analogous "determining that an application requires a plurality of [cores]" to run a multi-core application. *See* Responsive Br. at 24. The Court disagrees. Simply because the method of claim 20 runs a single core application upon identifying a single core task does create a parallel requirement out of thin air with respect to running a multi-core application. Nothing in the claim language mandates Intel's proposed limitation of "determining that an application requires a plurality of the multiple cores to run." *See* Responsive Br. at 24. Instead, the claim is silent on this point. Intel argues that the specification and prosecution history dictate that "multi-core applications are distinct from single-core applications" and must be handled "separately." *See id.* at 25 (citing '836 Patent at 9:65–10:3; 7/25/12 Amendment at 9, Ex. 12 to Selwyn Decl., ECF 158-13). The Court does not doubt the veracity of this statement—to handle multi-core and single core applications differently is a prime objective of claim 20. However, the Court finds nothing in the intrinsic record that requires the method of claim 20 to *determine* that an application requires a plurality of the multiple cores to run. Instead, for example, to run a multi-core application on a plurality of the multiple cores could be by default or pre-determined. The Court is simply not persuaded that Intel's proposed limitation is warranted over the surrounding claim language and presumption of plain and ordinary meaning, *see Thorner*, 669 F.3d at 1367.

Accordingly, the Court adopts the plain and ordinary meaning of the disputed term.

IV. ORDER

As set forth above, the Court construes the disputed terms as follows:

Claim Term	Court's Construction
"when in a second mode of operation" ('806 Patent, claim 11)	Plain and ordinary meaning, which includes the requirement of claim 11 that when in the second mode of operation the voltage(s) supplied to the first and second memory, respectively, must be lower than the minimum necessary for the first mode of operation
"arrangement of transistors" ('806 Patent, claims 6 and 11)	"arrangement of PMOS and/or NMOS transistors defined by the total number of transistors, number of PMOS or NMOS transistors, and manner of connection between the transistors"
"height" ('303 Patent, claims 1, 8, 11, 12, 18 and 19)	"physical dimension of distance from the base to the top of a structure in a direction substantially perpendicular to the primary surface"
"conversion controller coupled to the supply power converter" ('922 Patent, claims 1 and 11)	"conversion controller coupled to but separate from the supply power converter"
"estimated power loss" ('014 Patent, claims 1 and 12)	No construction necessary
"bumps . . . on top of the solder composition | solder interconnection layer" ('672 Patent, claims 3 and 12)	"solder bumps . . . on top of the solder composition | solder interconnection layer" where "on top of" includes the requirement that the solder bumps must be in contact with the solder composition | solder interconnection layer
"upon identifying a processing task that can not be run across the plurality of cores" ('836 Patent, claim 1)	"upon identifying a single-core task"
"upon identifying a processing task that cannot be run across the plurality of the multiple cores" ('836 Patent, claim 20)	"upon identifying a single-core task"
"a processing task that can not be run across the plurality of cores" ('836 Patent, claim 10)	"a single-core task upon identifying said task"

"running a multi-core application on a plurality of the multiple cores" ('836 Patent, claim 20)	No construction necessary

IT IS SO ORDERED.

Dated: February 15, 2019

BETH LABSON FREEMAN
United States District Judge

United States District Court
Northern District of California